What is claimed is:

1. A ferroelectric memory device comprising:

a memory cell array region;

a plurality of wordlines arranged in parallel to each other in a first direction within the memory cell array region;

a plurality of main bitlines arranged in parallel to each other in a second direction intersecting the first direction within the memory cell array region;

a plurality of blocks into which the memory cell array region is divided in the second direction;

a plurality of sub-bitlines provided for each of the main bitlines, each of the sub-bitlines being provided within one of the blocks;

a plurality of ferroelectric memory cells respectively provided at intersections between the sub-bitlines and the wordlines;

a plurality of first sub-bitline select switches respectively provided between the main bitlines and one ends of the sub-bitlines;

a common potential supply line which supplies a common potential to the sub-bitlines;

a plurality of second sub-bitline select switches respectively provided between the common potential supply line and the other ends of the sub-bitlines; and

a plurality of block select sections provided corresponding to the blocks,

wherein one of the block select sections selected from among the block select sections turns on the first sub-bitline select switches and turns off the second sub-bitline select switches in corresponding one of the blocks; and

wherein unselected block select sections among the block select sections turn off the first sub-bitline select switches and turn on the second sub-bitline select switches in corresponding two or more of the blocks.

2. The ferroelectric memory device as defined in claim 1,

wherein the common potential is substantially the same as an unselected wordline potential which is supplied to unselected blocks among the blocks.

3. The ferroelectric memory device as defined in claim 1,

wherein during a standby period in which no block is selected, the first sub -bitline select switches are turned off and the second sub-bitline select switches are turned on in all the blocks, and the common potential is substantially the same as a wordline potential during the standby period.

4. The ferroelectric memory device as defined in claim 3,

wherein potentials of the wordlines, the main bitlines, and the common potential supply line are set at the same potential during the standby period after turning the power on.

5. The ferroelectric memory device as defined in claim 4,

wherein the same potential is equal to the potential of the common potential supply line during an operation period.

6. A ferroelectric memory device comprising:

a memory cell array region;

a plurality of main wordlines arranged in parallel to each other in a first direction within the memory cell array region;

a plurality of bitlines arranged in parallel to each other in a second direction intersecting the first direction within the memory cell array region;

a plurality of blocks into which the memory cell array region is divided in the

first direction;

a plurality of sub-wordlines provided for each of the main wordlines, each of the sub-wordlines being provided within one of the blocks;

a plurality of ferroelectric memory cells respectively provided at intersections between the sub-wordlines and the bitlines;

a plurality of first sub-wordline select switches respectively provided between the main wordlines and one ends of the sub-wordlines;

a common potential supply line which supplies a common potential to the sub-wordlines;

a plurality of second sub-wordline select switches respectively provided between the common potential supply line and the other ends of the sub-wordlines; and

a plurality of block select sections provided corresponding to the blocks,

wherein one of the block select sections selected from among the block select sections turns on the first sub-wordline select switches and turns off the second sub-wordline select switches in corresponding one of the blocks; and

wherein unselected block select sections among the block select sections turn off the first sub-wordline select switches and turn on the second sub-wordline select switches in corresponding two or more of the blocks.

7. The ferroelectric memory device as defined in claim 6,

wherein the common potential is substantially the same as an unselected bitline potential which is supplied to unselected blocks among the blocks.

8. The ferroelectric memory device as defined in claim 6,

wherein during a standby period in which no block is selected, the first sub-wordline select switches are turned off and the second sub-wordline select switches are turned on in all the blocks, and the common potential is substantially the same as a

bitline potential during the standby period.

9. The ferroelectric memory device as defined in claim 8,

wherein potentials of the bitlines, the main wordlines, and the common potential supply line are set at the same potential during the standby period after turning the power on.

10. The ferroelectric memory device as defined in claim 9,

wherein the same potential is equal to the potential of the common potential supply line during an operation period.

11. A ferroelectric memory device comprising:

a memory cell array region divided into blocks in first and second directions intersecting each other;

a plurality of main wordlines arranged in parallel in the first direction within the memory cell array region;

a plurality of main bitlines arranged in parallel in the second direction within the memory cell array region;

a plurality of sub-wordlines provided for each of the main wordlines, each of the sub-wordlines being provided within one of the blocks;

a plurality of sub-bitlines provided for each of the main bitlines, each of the sub-bitlines being provided within one of the blocks;

a plurality of ferroelectric memory cells respectively provided at intersections between the sub-wordlines and the sub-bitlines;

a plurality of first sub-wordline select switches respectively provided between the main wordlines and one ends of the sub-wordlines;

a plurality of first sub-bitline select switches respectively provided between the

main bitlines and one ends of the sub-bitlines;

a first common potential supply line which supplies a common potential to the sub-wordlines;

a second common potential supply line which supplies a common potential to the sub-bitlines;

a plurality of second sub-wordline select switches respectively provided between the first common potential supply line and the other ends of the sub-wordlines;

a plurality of second sub-bitline select switches respectively provided between the second common potential supply line and the other ends of the sub-bitlines;

a plurality of first block select sections provided corresponding to the blocks divided in the second direction;

a plurality of second block select sections provided corresponding to the blocks divided in the first direction; and

a plurality of second block select sections provided corresponding to the plurality of blocks divided in the first direction,

wherein one of the first block select sections selected from among the first block select sections turns on the first sub-wordline select switches and turns off the second sub-wordline select switches in corresponding one of the blocks; and

wherein unselected first block select sections among the first block select sections turn off the first sub-wordline select switches and turn on the second sub-wordline select switches in corresponding two or more of the blocks.

wherein one of the second block select sections selected from among the second block select sections turns on the first sub-bitline select switches and turns off the second sub-bitline select switches in corresponding one of the blocks; and

wherein unselected second block select sections among the second block select sections turn off the second sub-bitline select switches and turn on the second sub-bitline select switches in corresponding two or more of the blocks.

12. The ferroelectric memory device as defined in claim 11,

wherein during a standby period in which no block is selected, the first sub -bitline select switches and the first sub-wordline select switches are turned off and the second sub-bitline select switches and the second sub-wordline select switches are turned on in all the blocks.

13. The ferroelectric memory device as defined in claim 12,

wherein potentials of the main wordlines, the main bitlines, and the first and second common potential supply lines are set at the same potential during the standby period after turning the power on.

14. The ferroelectric memory device as defined in claim 11,

wherein the first and second common potential supply lines are connected to different test terminals.

15. The ferroelectric memory device as defined in claim 13,

wherein the same potential is equal to the potential of the first and second common potential supply lines during an operation period.